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Dry etching technologies for next generation devices

Hisataka Hayashi[1], Katsumi Yamamoto[1], Toshiyuki Sasaki[1], Mitsuhiro Omura[1], Keisuke Kikutani[1], Itsuko Sakai[1], and Akio Ui[2]

[1] Toshiba Memory Corporation, [2] Corporate Research & Development Center, Toshiba Corporation

1. Introduction

As LSI device size shrinks, precise control of the fine pattern etching is required. Maximum ion energy in bimodal ion energy distribution due to the bias rf affected the etched pattern inaccuracy, and high rf reduced the maximum ion energy resulting in etched pattern accuracy [1]. Furthermore we have studied fine ion energy control using pulsed-DC superimposed (p-DCS) 100 MHz rf CCP. The ion energy distribution function (IEDF) of the p-DCS was compared with 13.56 MHz superimposed 100 MHz CCP (DFS CCP), and its effect on fine pattern etching [2].

2. Experimental

The 100 MHz rf power to generate plasma and 1 MHz negatively biased rectangular pulsed-DC voltage at 70% duty to accelerate positive ions were applied to the cathode. The DFS CCP was used as a reference [1].

The SOC (Spin-on Carbon) etch rates, the etched profiles of the SOC hole patterns with SOG (Spin-on Glass) as mask and the CD shift (as RIE – initial), were measured as a function of the pulsed-DC voltage (0 to 750 V) and the 13.56 MHz rf power (0 to 800 W). H_2 based gas chemistry was used.

3. Results and discussion

The IEDFs of the incident H_2^+ ions to the wafer were calculated based on the measured waveforms for both p-DCS and DFS [3]. In the p-DCS case (Fig. 1(a)), all the IEDFs except 0 V case showed the two sharp peaks profiles, and about 70% of the total ion flux was concentrated at the higher energy peak region. The ratio of the ion flux in the higher peak region to the total ion flux corresponded to the duty ratio of the pulsed-DC. In the case of 13.56 MHz (Fig. 1(b)), the IEDFs showed the bimodal shapes, and ion flux was widely distributed between two peaks. Maximum ion energy increased and IEDFs became broader with increasing rf power.

Next, the p-DCS CCP was applied to the SOC hole pattern etching. The SOC etch rates, the CD shift and the SOC etched profiles were shown in Fig. 2. The SOC etch rates in both of the 13.56 MHz and the pulsed-DC cases, increased with increasing superimposed power and voltage, respectively.

Under the 100 MHz single frequency CCP condition, large SOC undercuts below the SOG mask were observed, and the CD shift was 19 nm. In the p-DCS case, the CD shifts decreased with pulsed-DC voltage increase, and it decreased to 3 nm at the voltage of 750 V. In the case of 13.56 MHz, with increasing rf power, the CD shifts decreased to 9 nm at 400 W and then increased to 20 nm at 800 W, because the SOG mask severely eroded as shown in Fig. 2. The SOC etch rate at the 13.56 MHz power of 800 W was the same as that of the pulsed-DC of 750 V, but SOG mask erosion was different. It was supposed that erosion was enhanced by the higher ion energy of 740 V at the higher peak of 13.56 MHz case (Fig. 1(b)) compared to that of 510 V in the p-DCS case (Fig. 1(a)). SOG mask erosion was influenced severely by high energy ion bombardment. Fine ion energy control was the key factor for fine pattern etching. Highly concentrated ion energy distribution by p-DCS CCP was effective for SOC etch.

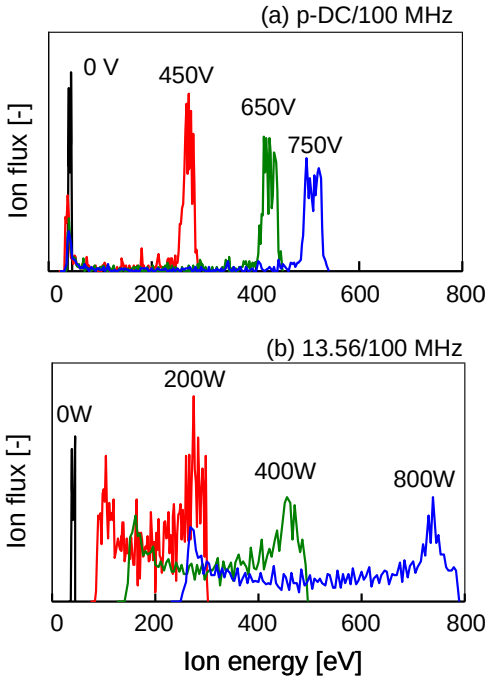

Fig. 1 IEDFs of H_2^+ ions for (a) the pulsed-DC / 100 MHz CCP and (b) 13.56 / 100 MHz CCP.

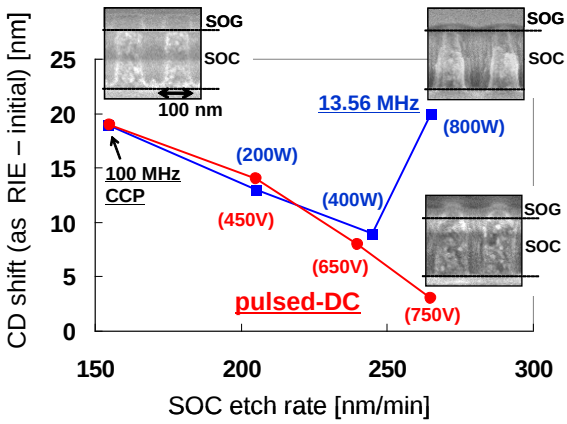

Fig. 2 CD shift as a function of SOC etch rate, and SEM images of SOC hole patterns.

References

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