Effect of Plasma Process Parameters on the Electrical Characteristics of Dual-Gate Graphene Field-Effect Transistors

Monika Verma[1], Suresh C. Sharma[1]
[1]Department of Applied Physics, Delhi Technological University, Bawana Road, Delhi-110042, India
e-mail (Presenter): monika_verma@live.com

Abstract
Graphene, a single layer of carbon atoms arranged in a hexagonal lattice, has emerged as a highly promising material in the semiconductor industry due to its remarkable carrier mobility, thermal stability, and adaptability for fabrication through chemical vapor deposition (CVD) techniques.[1] In conventional CVD, carbon-rich gases are introduced into a vacuum chamber at high temperatures (~1000°C), where they decompose and deposit carbon atoms onto a substrate to form graphene.[2] Among the variations of CVD, Plasma-Enhanced Chemical Vapor Deposition (PECVD) stands out for enabling graphene synthesis at significantly lower temperatures (~350°C). This is achieved by generating a high-frequency plasma (typically at 13.56 MHz), which provides the energy needed for gas decomposition without excessive heating, thus making PECVD more suitable for temperature-sensitive applications.

As Moore's Law drives the downscaling of transistor dimensions, silicon-based Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) face increasing limitations such as leakage currents, short-channel effects (SCE), and drain-induced barrier lowering (DIBL)[3]. These challenges have intensified the search for alternative channel materials, with graphene gaining attention due to its superior electrical and physical properties. Graphene Field-Effect Transistors (GFETs) are emerging as strong contenders in meeting the stringent performance needs of nanoscale electronic devices.

In this study, we have considered a semiconducting graphene sheet synthesized using the PECVD process, which is used as a channel in a dual-gate GFET structure designed using SILVACO TCAD software, based on our specifications. Our observations indicate that altering the physical properties of the graphene sheet—by varying plasma processing parameters such as electron/ion temperatures and electron/ion densities—significantly influences the device's electrical behavior.
Specifically, reducing the plasma parameters leads to improved electrical performance, evidenced by an increase in the Ion/Ioff ratio, drain current, transconductance, cutoff frequency, etc. These enhancements suggest that the device performs well in applications such as low-power, high-frequency signal processing and biosensing. Additionally, when the designed dual-gate GFET is compared with a conventional silicon-based FET, it exhibits superior electrical characteristics, highlighting its potential as a viable replacement for Si FETs in the ongoing trend of device miniaturization.

References
[1] A. K. Geim and K. S. Novoselov, The rise of graphene,Nature Materials, vol. 6, no. 3, pp. 183–191, (2007).
[2] R. Muñoz and C. Gómez-Aleixandre, Review of CVD synthesis of graphene, Chemical Vapor Deposition, vol. 19, no. 10-12, pp. 297–322, (2013).
[3] G. H. Nayana, P. Vimala, M. K. Pandian, and T. S. A. Samuel, Recent advancements in diamond-like carbon films: Properties and applications, Diamond and Related Materials, vol. 121, p. 108784, (2022)
[4] Bechhofer A, Ueda A, Teherani J, The 2D Debye length: An analytical study of weak charge screening in 2D semiconductors. Journal of Applied Physics 129(2), (2021).
[5] R. Vishnoi and M. J. Kumar, A Pseudo-2-D-Analytical Model of Dual Material Gate All-Around Nanowire Tunneling FET. IEEE Transactions on Electron Devices, vol. 61, no. 7, pp. 2264-2270, (2014).
[6] Simionescu O-G, Avram A, Adiaconiţă B, Preda P, Pârvulescu C, Năstase F, Chiriac E, Av-ram M. Field-Effect Transistors Based on Single-Layer Graphene and Graphene-Derived Materi-als. Micromachines. 14(6):1096 (2023).
[7] Suresh C. Sharma, Neha Gupta, Theoretical modeling of the plasma-assisted catalytic growth and field emission properties of graphene sheet. Physics of Plasmas 22, 123517 (2015).
[8] M. Kansal, Suresh C. Sharma, Plasma-based nanoarchitectonics for vertically aligned dual-metal carbon nanotube field-effect transistor (VA-DMCNFET) device: effect of plasma parameters on transistor properties. Applied Physics A, 128(1), 1-11 (2022).
[9] F. F. Chen, Introduction to Plasma Physics and Controlled Fusion, Vol. 1, 2nd ed., Springer, New York, NY (1984).
[10] S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd ed., McGraw-Hill, New York, NY (2003).