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Broadband MMIC Designs for Millimeter-Wave Plasma Diagnostics

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The designs of broadband microwave/millimeter-wave integrated circuits (MMIC's) by using GaN or CMOS semiconductor processes are crucial for the development of compact hot-electron plasma detection modules in both ECEI and MIR diagnostic systems. While the GaN-based circuits are more robust and can survive in harsh radiation environments, highly-sophisticated or the so-called SoC (System-on-Chip) circuits can be implemented by using CMOS technology. Different broadband integrated-circuit designs using TSMC 40/90-nm CMOS processes for both W- and D-band applications are therefore presented.

Fig. 1 is the layout of the W-band receiver where single-sideband functionality has been implemented to allow for image rejection over wide RF bandwidth; thus, improved spectra resolution and sensitivity can be obtained. The incoming RF signal will first be amplified by the 5-stage RF-LNA and sent to a broadband three-port RF quadrature coupler. The two RF-I/Q signals are then down-converted to IF-I/Q signals by a pair of double-balanced mixers. A 4-to-12 GHz four-port quadrature coupler then transform the IF-I/Q to separate upper-sideband and lower-sideband outputs. The LO chain is basically a frequency tripler and a two-stage driving amplifier. The image rejection ratio (IRR) will be larger than 15 dB in the simulation over the intended bandwidth. The RF-to-IF conversion gain is 30 dB and the overall noise figure is 10 dB. The chip size is 1.5 mm^2 and the total power consumption is less than 0.6 W under DC bias of 1.8 V.

Fig. 2 shows the layout of the double-sideband receiver in D-band which is made of 5-stage RF-LNA, a double-balanced mixer, IF amplification stage, LO tripler and driving amplifier. The overall RF-to-IF conversion gain is more than 15 dB, and the noise figure is close to 18 dB in the simulation. With 1.8 V bias, the power consumption is 0.5 W; the chip area is 0.9 mm^2. Here the RF upper frequency of 180 GHz is mainly constraint by the 40-nm CMOS process itself as considerable gain degradation is observed at much higher frequency. To better handle the output power range of the D- and W-band receivers, a 5-bit C/X-band variable gain amplifier (VGA) has also been designed by using 90-nm CMOS, as shown in Fig. 3, with incrementable gain step of 0.5 dB from 4 to 12 GHz. This VGA also serves as a band-pass filter for the IF signals.

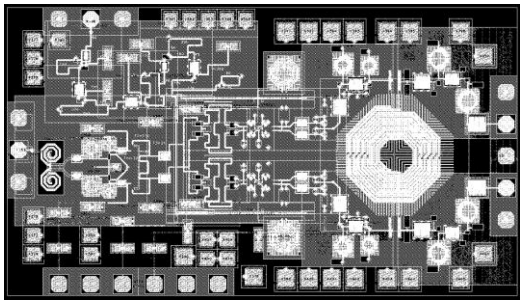

Fig. 1 W-band 40-nm CMOS receiver.

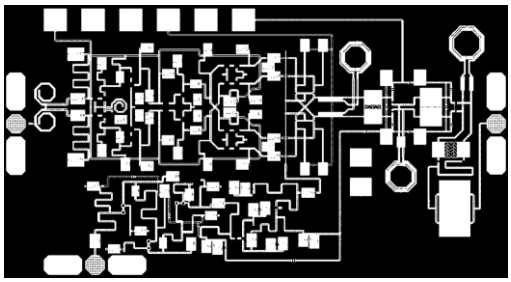

Fig. 2 D-band 40-nm CMOS receiver.

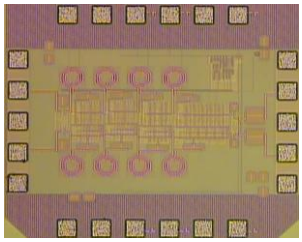

Fig. 3 C/X-band 90-nm CMOS VGA.